

1 INTRODUCTION to Multi Chip Modules

This chapter covers the different varieties of multichip modules. Chapter 1.1 to 1.7 is an introduction to the subject and is intended for those who want an overview of the technology. Part 2 cover each of the substrate technologies in more detail. The attachment and encapsulation technologies are covered in other parts of this guideline. Most of the material in the chapters; 2.2.1.1 to 2.2.1.5, 2.2.2.1 to 2.2.2.5 and 2.2.3.1 to 2.2.3.5 is with the authors permission taken from the book "*Electronic Components, Packaging and Production*" [1] by Leif Halbo and Per Øhickers.

1.1 What is Multi Chip Modules

A Multi Chip Modules, abbreviated "MCM", is described as a package combining multiple ICs into a single system-level unit. The resulting module is capable of handling an entire function. An MCM can in many ways be looked upon as a single component containing several components connected to do some function. The components are normally mounted un-encapsulated on a substrate where the bare dies are connected to the surface by wire bonding, tape bonding or flip-chip. The module is then personated by some kind of plastic moulding. The module is then mounted on the PCB in the same way as any other QFP or BGA component. MCMs offer an astounding variety of advantages instead of mounting packaged components directly on the PCB:

- Performance improvements, such as shorter interconnect lengths between die (resulting in reduced time of flight), lower power supply inductance, lower capacitance loading, less cross talk, and lower off-chip driver power
- Miniaturization, since MCMs result in a smaller overall package when compared to packaged components performing the same function, hence resulting I/O to the system board is significantly reduced
- Time-to-market, making them attractive alternatives to ASICs, especially for products with short life cycles
- Low-cost silicon sweep, allowing integration of mixed semiconductor technology, such as SiGe or GaAs
- Configuration as hybrids, including surface mount devices in the form of chip scale or micro-ball grid array (BGA) packages and discrete chip capacitors and resistors
- Simplification of board complexity by sweeping several devices onto one package, thereby by reducing total opportunities for error at the board assembly level, as well as allowing for a cheaper PCB
- Improved reliability by decreasing the number of interconnects between "components" and boards
- Adding new functions to a fixed footprint
- Capability of accommodating a variety of second-level interconnects. While BGA are the most popular, lead-frame solutions can be employed for plugability, enabling modularity for upgrades.

Although there is many good reasons for using MCMs, there are also some difficulties and disadvantages. The most important problem that hinders a more widespread use is the availability of components in "Bare Die" form. Although the market is improving, there is still a long way to go before most components are available as "Bare Dies". The other concern is cost. Although the newer MCM-L technologies have a low cost potential, cost is rarely the sole reason for going into MCMs.

There are three separate technologies involved in the manufacture of MCM:

1. Substrate technology
2. Die attach and bonding technology i.e. Wire-Bond, TAB or Flip-Chip
3. Encapsulation technology

Normally these items can be addressed separately.

1.2 MCM marked forecast

U.S. has been the primary consumer of MCMs, Figure 1 shows regional growth is shifting away from the U.S. and into Europe and Asia over the next five to seven years. This is primarily due to the growing telecom

need in Europe and the drive for miniaturisation in consumer products coming out of Japan. Both of these drive the need for lightweight solutions that are conservative on real estate consumption. Another significant trend is the migration to flip chip MCMs. Flip chip MCMs are expected to grow at 108% CAGR to comprise 18% of the MCM opportunity by 2001 [1]. These are indicators that known good die and an infrastructure for flip chip bumping are becoming a realisation.

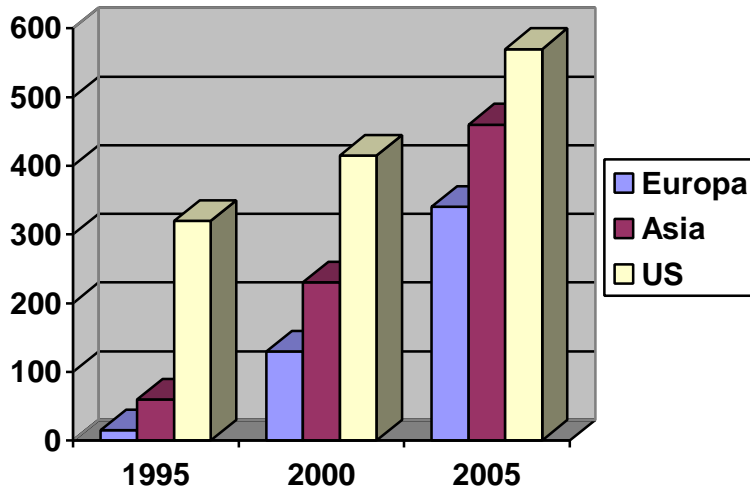


Figure 1. The data for MCM and MCP regional growth by revenue show that grow is shifting away from the U.S. and into Europe and Asia over the next five to seven years. Source: BPA Associates and Electronic Trends.

1.3 Choice of right technology

There are several aspects to consider when choosing the right technology for a multi chip technology. Below follows a discussion of some of them.

1.3.1 MCMs vs. ASICs

MCM designs are very practical when integration of mixed silicon technology is required. Silicon germanium is an enabler of high-frequency applications, such as global positioning systems and satellite systems operating in the GHz frequency range. For these designs, MCMs provide the integration required plus the benefit of a smaller overall package combined with performance. The best argument for using MCMs over ASICs, though, is time-to-market. MCMs can enable functional products to enter the marketplace several times faster than comparable ASIC designs. This is significant for prototype designs or products for competitive low-cost demand.

For products with longer life cycles, the total cost scenario must be analysed. Assembly yield considerations become significant for high-volume applications. Although MCMs have a low up-front cost compared with ASICs, factors such as die yield and assembly yield can keep costs high over the life of the product. The advantage of ASICs in this scenario would be the opportunity to spread the up-front engineering cost over the piece price and leverage the resulting high yield. In the case of an existing product where mature die is being utilised and product shrink is required, an MCM might make more sense. In many cases, the optimum solution might dictate the use of MCM technology to achieve acceptance, followed by an ASIC to support production volumes. Integration of silicon sometimes enables incorporating ASICs onto an MCM to combine memory and clock drivers to overcome the challenges of the speed limitations at the board level.

1.3.2 High frequency

The electrical performance of a package is mainly determined by the geometries and materials used in the package. If high frequency properties are important, a technology must be chosen that offers dielectrics with both low dielectric constant and low dielectric loss. The metal system must have high specific conductivity to minimise the conduction losses. At high frequency, the skin effect means that only the surface of the conductor contributes to the conduction. To obtain well-controlled characteristic impedance the technology must allow precisely defined conductor edges. This means that substrate and the added dielectric layers must have a smooth surface. Water absorption in organic dielectrics will cause a significant change in dielectric constant, changing the impedance of a line. In a harsh environment, this might imply that a circuit with organic dielectric has to be packaged in a hermetic package.

1.3.3 Thermal properties

For some applications, the thermal properties are important. The first way to improve the thermal properties is to choose a substrate with a good thermal conductivity, like certain ceramic materials (beryllium oxide or silicon nitride), silicon or metal based substrates. If the substrate itself is not able to cope with the power, alternative heat paths have to be found. This can be to attach the chips to some type of heat sinks, and use natural or forced convection principles to bring the die-temperature to the specified level.

1.3.4 Miniaturisation

If miniaturisation is the main goal, parameters like line width, line spacing and via-hole dimensions become very important. The type of electrical connection between the die and the substrate will also play a role, as both wire bonding and TAB needs certain spacing along the chip for the connection. Flip Chip technology on the other hand requires no extra area.

1.3.5 Cost

In many applications, cost is the main constraint. When discussing cost it is very important to consider the production volume, as some technologies will have a substantial "start up" cost. The way the total circuit is divided (or partitioned) into different sub modules will be very important for the total cost. Production yield and reparability will also have a mayor influence on the cost, as well as the problems associated with known good die (KGD).

The cost can be divided into substrate cost, which covers both the mechanical carrier as well as the conductor pattern. Both material cost and processing cost must be considered. The choice of encapsulation also has a big influence on the cost, and must be considered in connection with the environment in which the circuit is going to operate. Another important factor to consider is the test issue. This must be taken into account right from the module design.

1.4 Substrate Technology overview

The substrate forms the basis of the MCM and is the technology, which gets most attention. There exist an overwhelming amount of different technologies, each with its own set of advantages and disadvantages. To classify the different technologies, a division in the groups is often used based on the fabrication technique. The three techniques are Lamination, Deposition and Ceramic sintering.

1.4.1 MCM-L

Lamination based MCM's is today a very promising technology for many applications. Although greatly modified in some respects the MCM-L technologies is much based on the traditional printed circuit board technique where several layers of conductors and organic dielectrics are laminated together with pressure and heat cured. Several of the MCM-L technologies today are actually very fine-line printed circuit boards. Since these technologies have potential for low cost and high density, numerous variations of the technology are developed.

Advantages

- Low cost
- Medium to high packaging density
- Through visa for direct backside termination

Disadvantages

- Relative high coefficient of thermal expansion may cause problem when attaching large silicon chips.
- High moisture absorption put requirements on encapsulation.
- Low thermal conductivity implies more complex cooling design for power hungry IC's.

1.4.2 MCM C

Ceramic multichip modules are much of a classic in the MCM world. There are three main types; Thick Film, High Temperature Cofired and Low Temperature Cofired. All three are based on patterning by screen-printing where a ceramic or metal paste is pressed through a screen onto a substrate or a ceramic tape. The screen itself is manufactured with a photolithographic process from a film generated from the design data.

1.4.2.1 Thick Film

The thick film layers of conductors or dielectrics are added one at a time. After each layers is printed onto the ceramic base substrate, the substrate go through a drying stage, where the binder in the paste is burned off. The last stage is the firing which takes place at approximately 800 °C.

The main advantage of the thick film process is the relative simple process and cheap materials. Since this is a screen printing process, the minimum line width that can be printed is in the area of 100um. If narrower lines and spaces are needed, a combination of screen-printing and photolithography is used. The relative low firing temperature also allows a variety of metal pastes with a wide range of conductivities.

Advantages

- Low tooling cost implies acceptable prices, also for low volumes.
- Relative low coefficient of thermal expansion that is compatible with silicon.
- Medium to high thermal conductivity allows a simpler thermal design.

Disadvantages

- Low to medium packaging density
- Vias through base substrate are relatively large and must be pre-cut with a laser.

1.4.2.2 High Temperature Cofired Ceramic (HTCC)

As the name implies in this technology all the layers is fired at the same time under high temperature (approx. 1600°C). This is probably one of the most used ceramic technology and its main use today is in single chip packaging where high I/O IC's is mounted in a Pin Grid Array (PGA) or a Ball Grid Array (BGA). There are not many metals that survive 1600 °C firing so the chosen conductor material is Tungsten. This is however, a metal with relative low electrical conductivity, and therefore not too well suited for the inter-chip interconnect in MCMs. The high shrinkage during firing also makes small vias difficult.

The conductor patterns is added to a dielectric tape by screen printing after the via-holes are punched in the tape. The via-holes are also filled with conductive paste in the printing process. The layers are then stacked up, laminated under pressure and temperature, and at last fired in an oven at 1600 °C.

Advantages

- Low price at medium to high volumes
- Relative low tooling cost for low volume production, where a numerical punch can punch one via on one layer at a time
- At higher volumes a punch that punch all vias on one layer can be used
- High number of layers possible (>50)
- Easy to terminate with PGA, BGA or CQFP
- Very good thermal performance ($\lambda \approx 30 \text{ W/mK}$)

- Chip cavities for later hermetic sealing is possible
- Relative low coefficient of thermal expansion that is compatible with silicon

Disadvantages

- High dielectric constant of dielectric material ($\epsilon_r \sim 10$)
- Low conductivity of conductors
- Very difficult to make solid ground-planes due to problems with warpage
- High tooling cost
- High weight

1.4.2.3 Low Temperature Cofired Ceramic (LTCC)

As the name implies that this is the same process as the HTCC except that in this technology all the layers is fired at the same time under a relatively low temperature (approx. 800 °C). The low firing temperature enables the use of precious metals in the conducting layers. The dielectric has somewhat lower dielectric constant.

Advantages

- Low price at medium to high volume
- Relative low tooling cost for low volume production, where a numerical punch can punch one via on one layer at a time
- At higher volumes a punch that punch all vias on one layer can be used
- Easy to terminate with PGA, BGA or CQFP
- High number of layers possible (>50)
- Chip cavities for later hermetic sealing is possible
- Relative low coefficient of thermal expansion that is compatible with silicon

Disadvantages

- Medium to high dielectric constant of dielectric material
- Impossible with solid ground-planes due to warpage
- High tooling cost
- High weight
- Difficult shrinkage control result in poor dimensional control
- Low to medium thermal performance ($\lambda \approx 3 \text{ W/mK}$)

1.4.3 MCM D

Deposited MCMs are MCMs where the conducting layers are deposited on some sort of carrier, usually ceramic but also on silicon. The metal deposition is normally done by sputtering or evaporation in vacuum. After the deposition process the metallized surface is patterned by applying a photosensitive resist that after exposing and developing function as an etch resist. All metal not covered by the resist is removed. After the patterning of one layer, a dielectric coating can be applied. For organic dielectrics this are often done by spinning or spraying, whereas non-organic dielectrics are deposited by Chemical Vapour Deposition (CVD). Holes in the dielectric are opened by a similar photolithographic process and new layers can be added.

1.4.3.1 Classic thin-film

Classic thin-film hybrid technology is an example of a technique that fall into this technology. This technology is based on one thin gold signal layer on top of an alumina substrate. Crossovers are made by wire bonding. The backside of the substrate can be gold coated for the use as a ground plane.

Advantages

- Narrow lines possible.
- Low dielectric loss tangent (≈ 0.0001)

- Resistors and small capacitors can be integrated in the wiring
- Trimming of resistors is possible
- Good - very good thermal performance, depending on the substrate ($\lambda \approx 30\text{-}200 \text{ W/mK}$)

Disadvantages

- One layer may cause routing problems.
- Long bond wires for crossovers may be too inductive for some applications.
- 50 ohm lines will be as wide as the thickness of the substrate.
- High dielectric constant ($\approx 7\text{-}10$)
- Medium cost

1.4.3.2 Silicon thin film

Silicon thin film technology is a simpler version of the VLSI process, where conducting layers of aluminium, separated by layers of silicon dioxide is placed on top of a silicon wafer. Often older process lines designed for semiconductor fabrication is converted to MCM lines. Often one or two layers of polymer thin film is deposited on the top aluminium layer. The low thickness of the silicon dioxide compensates for the low thermal conductivity.

Advantages

- Very narrow lines is possible on the aluminium layers ($<2\mu\text{m}$)
- Narrow lines possible on additional polymer layers ($<10\mu\text{m}$)
- Small via holes, especially on the aluminium layers.
- Perfect thermal match to silicon semiconductors
- Very good / Good thermal performance (The low thickness of the silicon dioxide compensate for the low thermal conductivity of SiO_2).

Disadvantages

- No through vias, all contact pads must be at the top.
- Thin metal layers may force the use of wide lines due to high resistance.
- If topside ground planes are used, wide lines will have a very high capacitance due to the thin silicon dioxide layers.
- High cost substrate

1.4.3.3 Polymer thin film

Polymer thin film a technology where thin ($<15\mu\text{m}$) polymer dielectric films is deposited on a stable base substrate such as silicon or alumina. Thin ($2\text{-}5\mu\text{m}$) conductor films, usually copper, is then deposited and processed photolithographically. The lower dielectric constant of the polymers (Polyimide, BCB, etc) together with the $10\text{-}15\mu\text{m}$ thick dielectric make 50 Ohm lines more practical.

Advantages

- Narrow lines is possible ($\approx 10\mu\text{m}$)
- Small to medium via holes. ($10\text{-}50\mu\text{m}$)
- Better suited for 50 Ohm lines.

Disadvantages

- No through vias, all contact pads must be at the top.
- Poor thermal conductivity of the polymer limits the applicability for higher power devices.
- Difficult to go above two layers.
- High cost

1.5 Module Assembly Techniques

1.5.1 Wire Bond

Wire bonding is currently the dominant chip to substrate connection method. The chip is attached to the substrate with the bonding pads facing away from the substrate. Connecting wires (bond wires) made of gold or aluminium are then attached by welding on the chip pads, pulled to the substrate pads and again attached by welding. Details can be found in the wire-bond guide.

Advantages

- Well proven method with good yield
- Low cost for low to medium production volumes
- No special chip metallization required, chips are normally designed for wire bond
- Can also be used if a few extra crossovers is needed on the substrate
- Function well down to a pad-pitch of approximately 80µm

Disadvantages

- Relatively slow, one bond at the time
- The size and movement of the bond-head may restrict how closely chips can be placed
- Inductance of bond-wires may limit the use in extreme high frequency devices
- Bondable (pure) gold is normally required on the substrate

1.5.2 Tape Automated Bonding (TAB)

Tape Automated Bonding is a technique where the chip is attached to a polyimide tape prepared with copper conductors. This attachment called the inner lead bond is normally done at the wafer "Fab". The copper wires are connected to the pre-bumped chips by thermocompression bonding, typically all in one go (gang bonding). This, however, may cause cracks in the chip passivation and sometimes one and one lead is connected at the time to allow better control of the bonding. The chips are normally distributed on rolls.

In the assembly plant, the tape is cut in such way that the outer part of the conductors (leads) is exposed. The chip/film assembly is then aligned and soldered or glued to the substrate using conductive adhesive. Normally the cutting and bonding is done in one operation with a tool specially designed for the chip/film assembly. In some applications, a technique called "flip-TAB" is used. In this case, the chips are faced towards the substrate before bonding. This allows much shorter wires and therefore increased high-frequency properties as well as increased packaging density.

Because of the high tooling investments, this technique is mostly used in very high volume products such as watches and LCDs.

Advantages

- Well suited for very high volume production; all bonds in one operation and the chips is delivered on rolls or in cartridges.
- Good electrical performance especially if a tape with a separate ground plane is used.
- Fan-out on the tape makes it possible to mount chips with fine pad pitch on a substrate with a much larger pad pitch.

Disadvantages

- Different bonding tools must be used for different outer lead area dimensions
- Bonding tools are expensive
- TAB film must be specially designed for every chip type
- Normally the chips need special bumping and metallurgy, which prohibit the use of off the shelf chips
- Cross-talk may occur in single layer film at high frequency, especially if the length of the conductors on the film is large
- Inductance of long conductors on single layer films may cause problems in the power supply of power hungry chips

1.5.3 Flip-Chip (FC)

Flip Chip is a very interesting chip attachment technique that will be one of the dominant techniques. The chips are then placed upside down on the substrate, which have the same pad pattern as the chip. This technique requires the formation of bumps onto the chip pads. These bumps can be solder alloy balls or copper bumps in case of solder connections. A lot of effort is currently put into the use of adhesive flip-chip technology. When solder or isotropic conductive adhesive is used, an underfill typically of epoxy is applied on two of the edges of the chip and flows under the chip by the capillary force. This will significantly improve the reliability of the joint. In case of solder flip-chip, the whole process, including the underfill can be done in a modern SMT line.

Advantages

- Very high IO count possible by covering the whole chip area with pads
- Ultimately cheap when infrastructure is settled
- Self alignment under reflow ease registration requirements
- Ideal for high frequency applications due to very low contact inductance
- Work with modern SMT lines equipped for Flip-Chip

Disadvantages

- Require extra metallization on chips
- Difficult to get chips with bumps in low quantities
- Fine pad pitch will require fine pitch boards
- The underfill of epoxy is slow
- Big chips mounted on polymer substrates require underfill to survive thermal cycling
- Bear dies is difficult to test

1.6 Module Encapsulation Techniques

When using bare dies on a substrate the chips must normally be protected from the environment. The most common dangers for the bare chips are mechanical damage and moisture related corrosion. A flip chip with a proper underfill does not normally require extra encapsulation. A few of the most popular techniques is described below.

1.6.1 Dam Moulding

Dam moulding is a encapsulation technique where a high viscosity encapsulant is dispensed as a dam and then the dam is filled with a low viscosity encapsulant. The dam and contents is then cured.

Advantages

- Simple and easy adaptable
- Almost no tooling cost
- Low thermal stress under production
- Well suited for BGA type packages

Disadvantages

- Slow, not suited for very high production volumes
- High thermal resistance, cooling depends very much on substrate

1.6.2 Transfer Moulding

Transfer moulding is the high volume choice for encapsulation. A special moulding tool is designed for each module type. One or more modules are mounted on a contact-lead frame. The moulding tool is then clamped around each module only exposing the leads. A plastic mould is the injected under high temperature and pressure. The tool is cooled and the modules are ejected.

Advantages

- Fast, good for high volume production
- Cheap materials

Disadvantages

- Expensive tooling prohibit the use in low production volumes
- Expensive moulding equipment
- High thermal stress for the modules
- Best for modules with low to medium lead count
- High thermal resistance

1.6.3 Hermetic Casing

Hermetic casing is to put the chip inside a box with a welded lid. The box is welded in nitrogen atmosphere, to fill the box with nitrogen. To prevent leakage in the pin feed-throughs, hermetic glass sealing is used for every pin. The box (package) is normally made of gold plated Kovar. Traditionally this has been the only way to guarantee total hermeticity.

Advantages

- Guaranteed hermeticity
- Medium - low thermal resistance, depending on the substrate
- Good shielding properties

Disadvantages

- High cost
- High weight
- Only suited for low to medium pin-count modules

1.7 Testing issues

The strategy of testing of multi chip modules must be considered carefully before starting the design of a multi chip module. Because of the dense packaging, placement of test probes can be difficult.

1.7.1 Boundary scan

IEEE 1149.1 "Test Access Port and Boundary Scan Architecture" is a scan method for printed circuit boards. The memory elements which make the scan chain, are placed in the bonding pads of the integrated circuits (IC). Each IC also contains a small controller with which the user may control what to test. The intended use of B-Scan was interconnect test where a test pattern is imposed on the outputs of one IC, and the response is received at the input of another IC. The concept is also useful for other features like checking correct placement, starting and receiving results from component self-test, etc.

Advantages

- "Virtual pins" simplifies the in-circuit test fixture
- Gives easy access to confined areas on printed circuit boards
- Gives easy control of which part to test
- May be used to load programs into FPGA and Flash components

Disadvantages

- Not useful for testing complex components on the board
- Runs at low speed

- Requires long time to shift in and out test patterns and responses
- Requires that the used components have B-Scan integrated

1.7.2 Built-In Self Test (BIST)

BIST is mainly used on integrated circuits, but is also useful for printed circuit boards. The method solves the problem of testing isolated parts of the circuit, which otherwise is difficult to access for testing. The concept is to use linear feedback shift registers (LFSR) as a pseudo random pattern generator (PRPG) and a signature analyser (SA). The pattern generator requires a starting "seed" to generate the desired sequence of patterns. This may be loaded through a shift sequence, for instance by using B-Scan. The purpose of the signature analyser is to compress the response into one single word that is shifted out, for instance through B-Scan.

Advantages

- May be the only way to test embedded RAM, ROM, etc.
- Runs at system speed

Disadvantages

- Requires large space in IC's
- Requires extra components on printed circuit boards

1.8 Acronym list

The world of MCM's sports more acronyms than most other technology. Below is a table of the most used acronyms together with a short explanation.

Table 1 Acronym list MCM

Al ₂ O ₃	Aluminium Oxide, also called Alumina
AlN	Aluminium Nitride
ASIC	Application Specific Integrated Circuit
BCB	Benzocyclobutene (photoimageable dielectric)
BeO	Beryllium Oxide also called Beryllia
BGA	Ball Grid Array,
BIST	Built-In Self Test,
FC	Flip Chip,
HTCC	High Temperature Ceramic Carrier
KGD	Known Good Die, naked chips (dies) that is fully tested before shipment from factory
LCD	Liquid Crystal Display
LTCC	Low Temperature Ceramic Carrier
MCM	Multi Chip Module, a way of mounting several dies on one substrate and packaging it as a single component
MCM-C	Multi Chip Module using Ceramic materials
MCM-D	Multi Chip Module using Deposition technique
MCM-L	Multi Chip Module using Lamination technique
MCP	Multi Chip Package
PCA	Printed Circuit board Assembly, a PCB with mounted components.
PCB	Printed Circuit Board, a single or multilayer interconnection board for components
QFP	Quad Flat Pack,
SBU	Sequential Build Up
TAB	Tape Automated Bonding,
WB	Wire Bond