The Nordic Electronic Packaging Guideline

Chapter D: CSP

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Chip Scale Packaging (CSP) Technology

The information presented in this chapter has been collected from a number of sources describing CSP activities, both nationally at IVF and reported elsewhere in the literature. The most important of the former being the Chip Scale Packaging Task Force, an international multi-client programme carried out between 1996 and 1997 and a project work carried out by two students at Chalmers University of Technology..

D1. Introduction to CSP Technology

D1.1 Definition of CSP

Originally, CSP was the acronym for Chip Size Packaging but very few packages are of true chip size. Therefore, the acronym is today usually used for Chip Scale Packaging. According to IPC's standard J-STD-012, "Implementation of Flip Chip and Chip Scale Technology" <LINK to IPC>, a CSP shall have an area of no more than 1.2X the area of the original die size and is direct surface mountable [D1].

D1.2 Description of various types of CSPs

In contrast to most other package types, the name of the package type, "Chip Scale Packaging", contains no information about how the package is constructed, except for that it shall have approximately the same size as the chip. Therefore, CSPs include component types with probably more dissimilar characteristics than any two other IC package types clearly manifesting the inaccuracy to look at CSPs as a homogenous group. Some packages look like miniaturised BGAs which names like miniBGA and µBGA indicate. Others have leads which give them properties similar to conventional leaded packages such as PLCCs. For this reason, CSPs are often classified based on their structure. At least four major categories have been proposed [D2]. These are: flex circuit interposer, rigid substrate interposer, custom lead frame, and wafer-level assembly. Examples of packages of these categories are given in Figure D1.

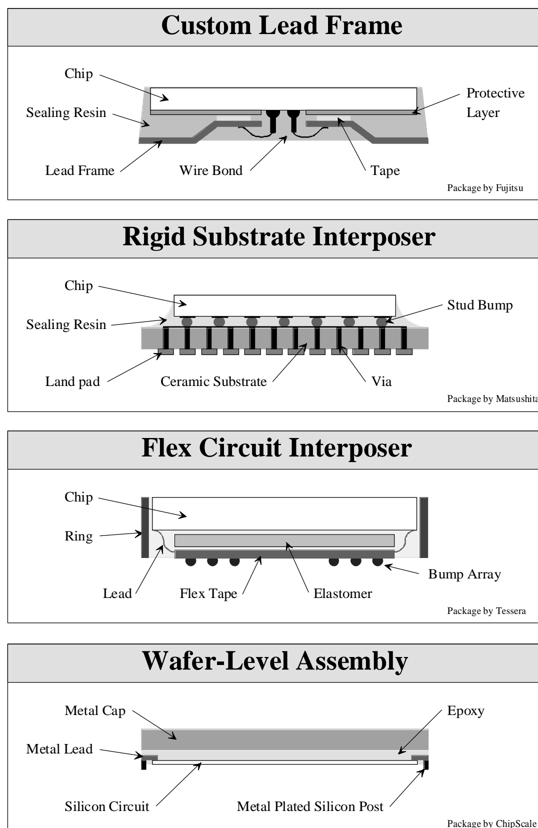

Figure D1. Main CSP Categories

D1.3 Driving Forces for using CSPs

The main driving forces for using CSPs are:

- Improvement in performance
- Size and weight reduction
- Easier assembly process (compared to bare die attach)
- Lower overall production costs.

Of these, reduction of size and weight are probably the most important factors for initial adoption of CSP technology. Consequently, consumer products like camcorders, mobile phones, and laptops are among the products that have been first to utilise CSPs.

D1.4 Advantages and disadvantages using CSPs

Chip Scale Packaging combines the best of flip chip assembly and surface mount technology. It gives almost the size and performance benefits as bare die chip assembly, at the same time as it offer the advantages of a encapsulated package. CSPs can be standardised, tested, surface mounted, and reworked. So far most CSPs have been produced for applications with rather low number of I/Os but many types of CSPs can be produced with large number of interconnections. However, before CSPs with large number of I/Os will find widespread use, techniques for producing reliable low-cost high-density printed boards must be developed.

The advantages and disadvantages of CSPs depend on what one compare with, standard surface mount or bare die assembly. Due to the large spread of characteristics for various CSPs, it also depend on the type of CSP.

<u>Advantages toward standard surface mount technology</u>

- Reduced package footprint
- Thin profile
- Reduced weight
- Better electrical performance
- Area array distribution of connections (for most CSPs)

<u>Advantages toward bare die assembly</u>

- Encapsulated package
- Testable
- Mountable with conventional assembly line
- Die shrinkable without changing footprint
- Some CSPs do not require underfill when mounted on organic substrates

<u>Disadvantages toward standard surface mount technology</u>

- Immature technology and poor infrastructure
- Limited availability
- Inspection of the solder joints is impossible without costly x-ray equipment
- Limited reliability data available
- Packages with high I/O counts require expensive high-density boards
- Rework more difficult
- Many CSPs require underfill when mounted on organic substrates
- Potential high cost

<u>Disadvantages toward bare die assembly</u>

- Somewhat inferior electrical and thermal properties

D1.5 Standards and Common Practice

The Institute for Interconnecting and Packaging Electronics Circuits (IPC) has released a standard dealing with CSP, J-STD-012 ”Implementation of Flip Chip and Chip Scale Technology” <LINK to IPC> [D1]. This standard contains technology overview and information on design considerations, material properties and processes, mounting and interconnection structures, assembly processes, requirements for reliability, and standardisation.

Although one of the advantages of CSPs compared to bare die assembling is the possibility to standardise, pitch and attachment site dimensions are still not standardised. Pitch and attachment site dimensions for grid array packages proposed by the Electronics Industry Association of Japan (EIAJ) is presented in Table D1.

Table D1. Proposed pitch and attachment site dimensions for grid array packages by the EIAJ.

Pitch (mm)	Attachment site diameter (mm)
0.4	0.25
0.5	0.30
0.65	0.40
0.8	0.50
1.0	

Tessera in USA has proposed 0.25, 0.50, 0.75, 1.00, and 1.25 mm as standard pitches and 0.10, 0.15, 0.20, 0.25, 0.30, and 0.35 mm as standard attachment site diameters for grid array packages.

For leaded packages, J-STD-012 prescribes that JEDEC’s publication JEP-95 should be followed which recommend the following pitches: 0.2, 0.3, 0.4, 0.5, 0.63, and 0.65 mm.

New standards that need to be developed are defined in J-STD-012. These standards, include the following:

- Std No. 102: Mechanical outline Standard for Flip Chip or Chip Scale Configurations
- Std No. 103: Performance Standard for Flip Chip/Chip Scale Bumps
- Std No. 104: Test Methods for Flip Chip or Chip Scale Performance
- Std No. 105: Flip Chip/Chip Scale Carrier Tray Standard
- Std No. 106: Bare Dice as Flip Chip or Chip Scale Configuration Management Standard
- Std No. 107: Design Standard for Flip Chip and Chip Scale Mounting Structures
- Std No. 111: Design Standard for Flip Chip/Chip Scale Assembly Configuration
- Std No. 112: Standard for Flip Chip/Chip Scale Assembly Performance Requirements
- Std No. 113: Test Methods for Qualification and Evaluation of Flip Chip/Chip Scale Assemblies
- Std No. 114: Standard for Flip Chip/Chip Scale Assembly Rework and Repair Techniques
- Std No. 115: Flip Chip/Chip Scale Assembly Reliability Standard
- Std No. 120: Qualification and Performance Standard for Flux used in Flip Chip Assembly

Some of these are now available as proposals (see Section D4.3) <Link>

D1.6 Price

Only a few CSPs are in production today and then in low volume production. Therefore, it is difficult to get information of what the price will be for various CSPs. Furthermore, the large variations in construction of the various package types will also affect the production costs for the various packages. Many company forecast that the cost initially will be 10 to 50 % higher than conventional packages and that cost parity will be reached when they are produced in high volumes.

D2. Conclusions and Guidelines

D2.1 Technical Issues

D2.1.1 Basic properties of CSP packages

A large number of CSPs have been described in the literature. Some key features for various CSPs are given presented in Table D2.

Figure D2. Data summarised for various CSSPs.

Company	Construction	Interconnect	Pad layout	I/O shape, type	No. of I/Os	Pitch (mm)
Amkor/Anam´s Chip Array Package	Rigid, BT resin	Wire bond, Au or Al	Array or peripheral	Eutectic solder balls or solder lands	Low to high	1.0
Amkor/Anam´s ChipSOP Package	Lead frame		Peripheral	Leadless	Low	
ChipScale Inc.'s Micro SMT Pack.	Wafer	Metal bridge	Peripheral	Lands	Low to medium	0.2 - 0.8
Citizen Watch's Fine-pitch BGA	Rigid, BT resin	Flip chip, solid core	Array	Eutectic solder balls	Medium to high	-
Fraunhofer/TU Berlin's Flex-based CSP	Flex	FPC	Array	Solder balls	Medium to high	0.5 - 0.8
Fujitsu´s SON Package	Lead frame	Wire bond	Peripheral	Lands	Low	0.5 - 1.0
Fujitsu´s Lead Frame Fine Pitch BGA	Lead frame, Cu core	Wire bond	Array	Solder balls	Medium to high	0.8
Fujitsu´s Lead Frame QFN Package	Lead frame	Wire bond	Peripheral	Solder plated lands	Low to medium	0.8
Fujitsu´s Resin-Bump SON CSP	Lead frame	Wire bond	Peripheral	Plated resin bumps	Low	0.8
Fujitsu´s FPC Fine Pitch BGA	Flex	TAB	Array	Solder balls	Medium to high	0.8
Fujitsu´s Ceramic Fine Pitch BGA	Rigid ceramic,	Wire bond or flip chip	Array	Solder balls	Medium to high	0.65 - 1.0
General Electric's TZOP	Flex	metallized laser vias	Array	Solder balls	Low to high	Custom
Hitachi Cable's LOC-CSP	Lead frame	Wire bond	Peripheral	J-lead	Low	0.3 - 0.65
Hitachi Cable's µstud BGA Package	Lead frame	Wire bond	Fan-out	Metal studs	Medium to high	0.5
LG Semicon's Bottom Leaded Plastic Package	Lead frame	Wire bond	Peripheral	Lands	Low	0.5 - 1.0
Matsushita's Ceramic CSP	Rigid, ceramic	Flip chip, stud Au, ICA	Array	Lands	Medium to high	1.0
Mitsubishi Electric's Molded CSP	Bumped, transfer moulding	Flip chip	Peripheral or array	Solder bumps on chip	Low to high	0.5 - 1.0
Motorola's JACS-PAC	Rigid, BT or FR-5?	Flip chip	Peripheral	Eutectic solder balls	Medium to high	0.5 - 0.8
National Semi.'s Plastic Chip Carrier	Rigid, laminate	Wire bond	Peripheral	Castellations	Low	-
NEC's Fine-Pitch BGA	Flex	single point TAB	Array	Solder balls	Medium to high	0.5
Nitto Denko's Resin Molded CSP	Flex	Flip chip	Array	Solder balls	Low to high	Custom
Oki Electric's CSP	Rigid, polyimide	Flip chip	Array	Solder balls	Medium to high	0.8
Rohm's TCP-based CSP	Lead frame	TAB	Peripheral		Low	0.5
Sharp's F.BGA Package	Flex	Wire bond, Au	Array	Eutectic solder balls	Medium to high	0.8 - 1.0
ShellCase's Shell-BGA Package	Wafer	Thin film	Array	Solder balls	Low to high	0.25 (min)
Silicon Systems' ULTP	Rigid, BT	Wire bond	Peripheral	Lands	Low to medium	0.5
Singapore's IME's CSP	Bumped, transfer moulding	Bumped chip	"Array"	Solder balls	Low to medium	-
Tessera's µBGA Package	Flex, elastomer	TAB leads	Array	Solder balls	Low to high	0.25 - 1.0
Toshiba's CSTP	Rigid, ceramic or laminate	thermo-compression gold-to-gold	Array	Lands or eutectic solder balls	Medium to high	0.8 - 1.0
Toshiba's Fan-Out FBGA Package	Rigid, ceramic	Wire bond	Array	Solder balls	Medium to high	0.5 - 0.8

TI Japan's Microstar BGA	Flex	Wire bond (Flip chip future)	Array	Eutectic solder balls	Medium to high	0.5 - 0.8
3-D Plus Flip-Chip CSP	Wafer	Wire bond	Peripheral	Lands	Low to medium	-

D2.1.2 Electrical performance

A comparative table of various technologies for a 100 lead 10x10 mm die is given in Tables D3 and D4 including dimensional and electrical properties.

Table D3. Comparative figures for various technologies (from Ref. D1).

Feature	Bare die (wire bonded)	Flip chip	QFP	μBGA	Micro SMT
Pitch (mm)	0.15	0.25	0.30	0.50	0.30
Footprint area (mm2)	125	120	785	150	110
Ratio of package to die	1	1	6.30	1.20	1.10
Height (mm)	0.4 - 0.6	0.5 - 0.70	1.4	0.84	0.3 - 0.5
Inductance (nH) (circuit length)	1 - 2 (0.75 mm wire)	0.1 - 0.2 (0.5 mm bump)	1 - 7 (0.7 - 3 mm wire and lead)	0.5 - 2.1 (1 mm bump)	0.1 - 0.2 (0.5 mm post and bridge)
Capacitance (pF)	0.2	0.03	0.5 - 1	0.05 - 0.2	0.02 - 0.03
PCB attachment	wire bond	solder	solder	solder	solder

Table D4. Comparative figures for various technologies (from Ref. D4)

Manufacturer	Package	Inductance (nH)	Capacitance (pF)
ChipScale	Micro SMT	0.1 - 0.2	0.02 - 0.2
Fujitsu	MF - LOC	0.3 - 2.4	n.a.
NEC	Fine-pitch BGA	0.3 - 2.3	0.05 - 0.34
ShellCase	ShellCase	<0.07	<1
Tessera	μBGA	0.5 - 2.1	0.05 - 0.2
Amko/Anam	PowerQuad2 MGFP	6 - 7	0.5 - 1.0
IBM	Cavity-down PGA	7.7 - 15.2	1.1 - 2.7
IBM	TapeBGA	1.3 - 5.5	0.4 - 2.4
IBM	Die-up BGA	1.5 - 8.0	0.2 - 1.0
IBM	Cavity-down BGA	1.7 - 8.3	0.2 - 0.9

D2.1.3 Thermal performance

Due to the construction of many CSPs, the junction-to-case thermal resistance of a CSP is usually lower than that of a conventional plastic package. However, due to the small size, the junction-to-ambient thermal resistance is greater. According to Steve Greathouse at Intel [D4], CSPs can handle die that dissipate 0.5 to 2 watts depending on type and materials used. At higher power dissipation, heatsinks, heatspriders, thermal vias in the boards, increased airflow, or other options must be used. This will increase the overall size requirements considerably which may lead to that size and cost savings may be lost. Table D5 shows some techniques for heat dissipation.

Table D5 CSP heat dissipation techniques [D3].

Company	Technique	Exposed IC back	Heat spreader	Metal lid	Plastic encap.
ChipScale	Back of IC exposed on board side	O			
Fujitsu	Back of IC exposed or metal heat spreader exposed	O	O		
General Electric	Back of IC exposed or plasric encapsulation on back of IC	O			O
Hitachi Cable	Molded LOC or heat spreader		O		O
IBM	Back of IC exposed or metal can	O		O	
LG Semicon	Plastic ancapsulation				O
Matsushita	Back of IC exposed	O			
Mitsubishi Electric	Plastic encapsulation				O
Motorola	Back of IC exposed	O			
NEC	Back of IC exposed	O			
Nitto Denko	Back of IC exposed or plastic encapsulation	O			O
Rohm	Back of IC exposed	O			
Sandia National	Back of IC exposed	O			
ShellCase	Optional AIN wafer sandwich		O		
Tessera	Back of IC exposed or metal can	O		O	
Toshiba	Back of IC exposed	O			

D2.1.4 Reliability issues

Qualification of packages are normally performed according to a number of standardised tests, such as those found in MIL-STD-883 [D5] and JEDEC Standard No. 22 [D6]. Some of the most used tests are listed in Table D6.

Table D6. Common tests used for qualification of packages [D3].

Test	Conditions	Duration
Thermal shock	-55°C to +125°C, Method A110	100 cycles
Thermal cycling	-55°C to +125°C	1,000 cycles
Pressure pot	121°C, 100% RH, 2 atmospheres	168 hours
HAST (Highly Accelerated Stress Testing)	130°C, 85% RH, 5.5V bias	96 hours
High temperature storage	150°C	1,000 hours
Mechanical shock	600G, 2.5 msec, Method 2002	6 axis
Solderability	JEDEC 22-B	
Physical dimensions	JEDEC 22-B	
Mark permanency	JEDEC 2015	

Published results from qualification testing of various CSPs are given in Table 7D.

Table D7. Published results from qualification testing of CSPs [D7].

Supplier	Package	Test	Test Conditions	Failure #/N
Intel	4 Mb Flash Structure = µBGA™	Temp. cycle B (FR4 interposer)	-55 to +125ºC, 1,000 cycles	0/78
	I/O = 46	Temp. cycle C (ceramic interp.)	-65 to +125ºC, 1,000 cycles	2/78 (4 WBs failed)
	Pitch = 0.7 mm	THB (ceramic interp.)	85ºC/85% RH, 1,000 hrs	0/78
	Size = 3.75 mm x 5.25 mm approx.	HAST (ceramic interp.)	130ºC/85% RH, 150 hrs	0/28
		Level 1 precond. (pkg)	85ºC/85% RH, 168 hrs	No delamination or crack
		High temp. storage (pkg)	150ºC, 1,000 hrs	0/78
Fujitsu	16 Mb DRAM Structure = SON	Temp. cycle test	-65 to +150ºC, 1hr/cycle, >500 cycles	0/40
	I/O = 26	Package crack (pkg)	85ºC/85% RH, 168 hrs, heat up to 245ºC	0/100
	Pitch = 1.0 mm Size = 7 x 16 mm	Temp. cycle test (pkg)	-65 to +150ºC, 500 cycles	0/25
		PCT (pkg)	121ºC, 2 atm. press, 100% 336 hrs (pre-cond.: 85ºC/85%, 168 hrs + IR)	0/25
Hitachi Cable	DRAM Structure=TAB tape-based CSP	Temp. cycle test	-55 to +125ºC, 1,500 cycles	0/21
	I/O = 40	High temp. and humidity (pkg)	85ºC/85% RH, 408 hrs	0/19
	Pitch = 1.0 mm	PCT (pkg)	121ºC, 2 atm. press., 480 hrs	0/41
	Size = 11.5 mm x 6.6 mm	High temp. storage (pkg)	150ºC, 1,000 hrs	0/11
LG Semicon	Test chip Structure=BLP	Temp. cycle test	-30 to +85ºC, >1,200 cycles	0/??
	I/O = 20	Preprocessing (pkg)	85ºC/85% RH, 168 hrs	No delamination or crack
	Pitch = 0.5 mm Size = 11.72 mm x 5.21 mm	Thermal shock (pkg)	IR reflow at 240ºC, 3X	No delamination or crack
Mitsubishi	Test Chip Structure=MCSP	Temp. cycle test (96 MCSP)	-40 to +125ºC, 1 hr/cycle, 200 cycles	0/20
	I/O = 96 (6 x 16)		(500 cycles)	(8/20)
	Pitch = 0.8 mm Size = 6.35 x 15.24 x 0.65 mm	High temp. and humidity (pkg) (1024 MCSP)	85ºC/85% RH, 48 hrs, heat to 235ºC max.	No delamination or crack (0/5)
Sharp	Test chip	Temp. cycle test	-40 to +125ºC, 300 cycles	0/18
	I/O = 160	High temp. and humidity	85ºC/85% RH, +7.0 V, 1000 hrs	0/25
	Pitch = 0.8 mm Size = 12 x 12 mm	Repeated bending test (Bd Size = 100 x 50 x 0.6 mm)	The mounted position is fulcrum. Bend 2 pts. on bd. w/2 mm deformation. 300 cycles.	0/10
	Structure = PI/Cu	Package crack (pkg)	30ºC, 75% RH, 96 hrs; heat to 230ºC, 2 cycles; PCT (121ºC, 1 atm., 100% RH), 300 hrs	0/32

During recent years, the traditional way of qualifying components has been questioned since it has become evident that it is not enough for assuring reliability of products using new technologies. For qualification of packages, JEDEC has published a standard entitled ”Failure-Mechanism-Driven Reliability Qualification of Silicon Devices” [D8] which is presented as an alternative to traditional stress-driven qualification. It is pointed out that in order for the standard to reach its full effectiveness, the original equipment manufacturers (OEM) and the supplier must develop partnerships. The OEM should accept the reliability qualification process performed by the supplier, per the guidelines of the standard, in lieu of the specific (special) reliability qualification process that many OEMs require today. The key issues in this process are to

identify the crucial failure mechanisms (physics-of-failure) that will determine the reliability of a CSP and how to appropriately accelerate these failure mechanisms in reliability tests. Since reliability testing has to be application specific, it will not be possible to have a number of fixed reliability tests to chose between for reliability evaluations. In most cases, existing test methods have to be altered in order to be adequate or new test methods have to be developed.

Furthermore, the very large variation of technologies used for constructing chip scale packages make it impossible to handle CSPs as a homogenous group when discussing reliability aspects. Since many of the technologies used are newly developed and unproved, one can expect that new types of failure mechanisms will arise for many of the package types. Since for most applications, the major reason for failures is the large difference in coefficients of thermal expansion (CTE) between silicon (chip) and printed board substrates, another classification than the previously described will be used when discussing reliability aspects of various CSPs in this section. It is based on how the design of the packages will affect stress distribution and failure mechanisms due to CTE mismatches between silicon and printed board substrate. This will, of course, also be affected by the type of printed board substrate used. If ceramic boards are used, the difference in CTE between the chip and the ceramic substrate will be small but, of cost reasons, this is not a viable alternative for most applications.

Components with leads

There are a few CSPs having leads, for example Hitachi Cable's LOC-CSP [D9]. The leads will provide compliance that will decrease the stresses of the solder joints and the connections inside the package. The amount of stress reduction will depend on the stiffness and configuration of the leads. The basic feature of the LOC-CSP is similar to a PLCC component and it can therefore be expected to have good reliability properties, especially since it is intended for low I/O counts, i.e. small dimensions. There will be no need to use underfills to improve reliability.

Packages with rigid structure and solder lands

The most typical characteristics of this type of package are the rigidity and the very low CTE. Examples are Matsushita's CSP [D10] and Toshiba's CSTP [D11] with solder lands, both using ceramic substrates. Also ShellCase's Shell-BGA [D12] with solder lands can be included in this package type. The rigid structure of these packages and the very low stand-off will cause extremely high stresses of the solder joints when exposed to temperature changes if they are soldered to organic printed boards. Therefore, they will mainly be used on ceramic printed boards. Packaged with small dimensions may be used on organic substrates for applications used in less demanding conditions. Use of underfill may extend the application fields.

Packages with organic structure and solder lands

This type of packages have solder lands created either by molding a lead frame into a resin or by plating the solder lands onto an organic laminate material. As for the package with rigid structure, high stress levels can be expected in the solder joints between packages and printed boards, but the organic resin in the package will give some flexibility to the package that will reduce the stresses in the solder joints somewhat. However, this will cause that cracking may also occur within the packages and the printed boards when organic boards are used. For this reason, the package type will only be suitable for small sizes, i.e. low number of I/Os, and less demanding conditionings. Use of underfill will improve reliability. Example of packages of this type are Amkor/Anam's ChipSOP™, Express Packaging Systems' NuCSP [D13], Fujitsu's SON package [D14], LG Semicon's BLP [D15], National Semi's PCC [D16], and Silicon Systems' ULTP [D17]. All these packages have terminals located along the periphery of the packages.

Packages with ceramic interposer and solder balls

This type of package is similar to the packages with rigid structure and solder lands, except for that the use of solder balls gives a higher stand-off for these packages that will improve reliability. The use of a ceramic interposer will prevent that stresses are distributed into the package. Still, the large difference in CTE for ceramic materials compared to organic laminate materials will make the use on organic printed boards questionable for demanding conditions. Example of packages of this type are IBM's Ceramic Mini Ball Grid Array package [D18], Fujitsu's Ceramic fine Pitch BGA, Toshiba's Fan-Out FBGA packages, and Kyocera's ceramic CSP [D19].

Packages with organic rigid interposer and solder balls

This type of packages has basically the same construction as Motorola´s OMPAC version of plastic BGA, except for the smaller dimensions. The chip is mounted on a laminate substrate, either using wire-bonding or flip chip techniques. The solder balls on the package will give some stand-off to the components that will result in an improved reliability compared to packages with solder lands. Also, the organic interposer will give some flexibility that will give a better reliability of solder joints compared to packages using ceramic interposers. On the other hand, the flexibility of the interposer will lead to an increased risk for connection failures inside packages. Amkor/Anam's Chip Array™ Package with solder balls, Citizen Watch's Fine-Pitch BGA, Motorola's SLICC [D20] and Oki Electric's CSP are examples of this package type.

Packages with flexible interposer and solder balls (rigid structure)

This package type shows large similarities with the previous package type except for that a flexible interposer is used instead of a laminate. In some packages, wire bonding is used in order to make the connection to the chip, for example Sharp's CSP [D21] and TI Japan's Microstar BGA™. However, many packages are using new innovative methods for creating the connection to the chip which may result in the appearance of new failure mechanisms that must be considered when evaluating the reliability. Package with new interconnection methods are Fraunhofer/TU Berlin's Flex-based CSP, General Electric's TZOP [D22], NEC's Fine-Pitch BGA [D23], Nitto Denko's Resin-Molded CSP [D24], and Sandia's mBGA [D25].

Packages with compliant layer

In order to reduce the stress on the solder joints, some packages are constructed with a compliant layer. The most well-known package of this type is Tessera's µBGA [D26],, but also ShipScale Inc.'s Micro SMT Package [D27] and EPIC technologies' EPIC CSP™ [D28] can be incorporated in this package type. The compliant layer will result in low stress levels of the solder joints making the use of underfill unnecessary even in rather harsh conditions. However, that is on the expense of increased movements in the compliant layer that leads to increased risk for failures within the package.

Moulded chips with solder balls

Mitsubishi Electric's Moulded CSP [D29] and Singapore's Institute of Microelectronics' CSP [D30] consist of bumped chips that have been plastic moulded. Solder balls have then been attached to the bumps. The similarity of these packages to flip chip is large. However, the larger stand-off for these packages will give better reliability than flip chip. Despite that, underfill will probably be necessary for many applications in order to get acceptable reliability.

Packages with metallised polymeric bumps

An increased stand-off can be achieved by using metallised polymeric bumps or posts on the package. It is an interesting to give compliancy to the connections but have only been achieved along the periphery of components. The limited experience of this type of connections make it difficult to predict the reliability and dominant failure mechanism. Example of packages of this type of packages are Fujitsu's Resin-Bump SON CSP [D31] and 3-D Plus' Plip-Chip CSP [D32].

Packages with metallic bumps

Some packages have what could be characterised as metallic bumps or studs, for example Fujitsu's Micro BGA and Lead Frame QFN packages [D33], and Hitachi Cable's µstud BGA Package. These packages are very disparate and, as for the previous group, difficult to predict the reliability and dominant failure mechanism.

D2.2 Production Issues

D2.2.1 Design rules and compatibility

Since only a few companies are using CSPs in their products, little experience is available about production issues. For CSPs with grid array structures, some of the experience gained from BGA technology is valid. However, for CSPs with small pitches and/or large number of I/Os, routing will be difficult. Some extra space can be gained by using via-in-pad. However, for many application areas, it will be necessary to use high-density boards such as microvia boards.

J-STD-012 recommend to use solder mask defined lands [D1]. Solder mask defined lands have been found to reduce reliability of BGAs <Link to BGA Chapter>. No studies have been reported of how they affect the reliability of CSPs.

For some CSPs without a compliant structure, it will be necessary to use underfill in order to get acceptable reliability when mounted on organic printed boards.

D2.2.2 Assembly Issues

Most CSPs can be mounted using current fine pitch SMT assembly materials and processes. Vision systems may have problem recognising the structure of some CSPs. In addition, some packages are moisture sensitive. That is, they must be stored in dry conditions and used within a specified time frame after they have been exposed to humid environments. If the time frame is surpassed, or if a package needs to be reworked, it should be baked before any work is performed.

In general, the same criteria is applicable for CSPs as for BGAs and QFPs <link to BGA Chapter>.

D2.2.3 Tools and investments

As pitches for CSP may get smaller conventional pick & placement machines may not suffer for mounting of the components which then will necessitate investments in new machines. Also, X-ray equipment my be necessary for inspection for verification of solder joints. In cases when underfills must be used of reliability reasons, material and equipment for the underfilling process will add to the total cost. See also the BGA Chapter. <link>

D2.2.4 Inspection and Workmanship Standards

Generally the same apply to CSPs as for BGAs (See the BGA Chapter <link>).

D2.2.5 Rework and Repair

Generally the same apply to CSPs as for BGAs (See the BGA Chapter <link>).

D3. Background Information

Please double-click on the items below to open the files in Adobe Acrobat Reader Format (.pdf).

D3.1 Report

V. Lundstedt och P-Å Svensson , Projektarbete EP/CTH-9704, CSP – Chip Scale Packaging, (in Swedish) <link>.

D4. References

D4.1 Recommended Readings

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P.-E. Tegehall, ”A Test strategy to verify the Reliability of Chip-Scale Packages”, Chip Scale Review, Nov 1998, pp. 73-81.

D4.2 Other References

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D4.3 Standards

J-STD-012, Implementation of Flip Chip and Chip Scale Technology, The Institute for Interconnecting and Packaging Electronics Circuits (IPC), January 1996.
J-STD-020, Moisture/Reflow Sensitivity Classification of Plastic Surface Mount devices, October 1996.

Official representative proposal
J-STD-027, Mechanical Outline Standard for Flip Chip or Chip Scale Configurations
J-STD-028, Performance Standard for Flip Chip/Chip Scale Bumps
J-STD-029, Test Methods for Flip Chip or Chip Scale Products
J-STD-030, Qualification and Performance of Flip Chip Underfill Materials
J-STD-031, Mechanical Outline Standard for Ball Grid rays and other High Density Technology
J-STD-032, Performance Standard for Ball Grid Array Bumps and Columns

Working Draft
J-STD-033, Packaging and Handling of moisture Sensitive Non-Hermetic Solid State Surface Mount Devices
J-STD-035, Acoustic Microscopy for Non-Hermetic Encapsulated Electronic Components
IPC-7076, Sectional Requirements for Chip Scale and Chip Size Component Mounting

D4.4 Conferences

Surface Mount International: http://www.surfacemount.com
IPC National Conferences: http://www.ipc.org/html/framesetEAEexpo.html
SEMI Technical Proceedings: http://www.semi.org
NEPCON: http://nepcon.reedexpo.com
CHIPCON: http://www.semitech.com/chipcon/index.html
APCON: http://www.semitech.com/apcon/index.html

D4.5 Companies

Amkor/Anam: http://www.amkor.com/assembly_and_test/products/chipscale/index.htm
ChipScale Inc.: http://www.chipscale.com
Flip Chip technologies: http://www.flipchip.com/electron.htm
Fujitsu: http://www.fujitsu.co.jp/hypertext/Products/Device/CATALOG/AD81/81-00001/8e-2.html
Hitachi Cable: http://www.hitachi-cable.co.jp/microbga/index.htm
Kyocera: http://www.kyocera.com/kai/csp.html
LG Semicon: http://www.lgs.co.kr/pkgdev/index.html
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