

Chip Scale Packaging (CSP) Technology

The information presented in this chapter has been collected from a number of sources describing CSP activities, both nationally at IVF and reported elsewhere in the literature. The most important of the former being the Chip Scale Packaging Task Force, an international multi-client programme carried out between 1996 and 1997 and a project work carried out by two students at Chalmers University of Technology..

D1. Introduction to CSP Technology

D1.1 Definition of CSP

Originally, CSP was the acronym for Chip Size Packaging but very few packages are of true chip size. Therefore, the acronym is today usually used for Chip Scale Packaging. According to IPC's standard J-STD-012, "Implementation of Flip Chip and Chip Scale Technology" <LINK to IPC>, a CSP shall have an area of no more than 1.2X the area of the original die size and is direct surface mountable [D1].

D1.2 Description of various types of CSPs

In contrast to most other package types, the name of the package type, "Chip Scale Packaging", contains no information about how the package is constructed, except for that it shall have approximately the same size as the chip. Therefore, CSPs include component types with probably more dissimilar characteristics than any two other IC package types clearly manifesting the inaccuracy to look at CSPs as a homogenous group. Some packages look like miniaturised BGAs which names like miniBGA and μ BGA indicate. Others have leads which give them properties similar to conventional leaded packages such as PLCCs. For this reason, CSPs are often classified based on their structure. At least four major categories have been proposed [D2]. These are: flex circuit interposer, rigid substrate interposer, custom lead frame, and wafer-level assembly. Examples of packages of these categories are given in Figure D1.

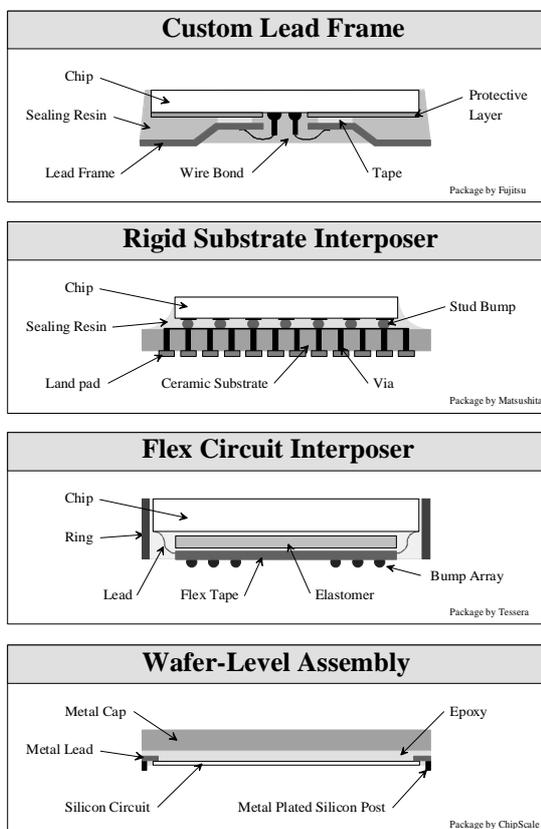


Figure D1. Main CSP Categories

D1.3 Driving Forces for using CSPs

The main driving forces for using CSPs are:

- Improvement in performance
- Size and weight reduction
- Easier assembly process (compared to bare die attach)
- Lower overall production costs.

Of these, reduction of size and weight are probably the most important factors for initial adoption of CSP technology. Consequently, consumer products like camcorders, mobile phones, and laptops are among the products that have been first to utilise CSPs.

D1.4 Advantages and disadvantages using CSPs

Chip Scale Packaging combines the best of flip chip assembly and surface mount technology. It gives almost the size and performance benefits as bare die chip assembly, at the same time as it offer the advantages of a encapsulated package. CSPs can be standardised, tested, surface mounted, and reworked. So far most CSPs have been produced for applications with rather low number of I/Os but many types of CSPs can be produced with large number of interconnections. However, before CSPs with large number of I/Os will find widespread use, techniques for producing reliable low-cost high-density printed boards must be developed.

The advantages and disadvantages of CSPs depend on what one compare with, standard surface mount or bare die assembly. Due to the large spread of characteristics for various CSPs, it also depend on the type of CSP.

Advantages toward standard surface mount technology

- Reduced package footprint
- Thin profile
- Reduced weight
- Better electrical performance
- Area array distribution of connections (for most CSPs)

Advantages toward bare die assembly

- Encapsulated package
- Testable
- Mountable with conventional assembly line
- Die shrinkable without changing footprint
- Some CSPs do not require underfill when mounted on organic substrates

Disadvantages toward standard surface mount technology

- Immature technology and poor infrastructure
- Limited availability
- Inspection of the solder joints is impossible without costly x-ray equipment
- Limited reliability data available
- Packages with high I/O counts require expensive high-density boards
- Rework more difficult
- Many CSPs require underfill when mounted on organic substrates
- Potential high cost

Disadvantages toward bare die assembly

- Somewhat inferior electrical and thermal properties

D1.5 Standards and Common Practice

The Institute for Interconnecting and Packaging Electronics Circuits (IPC) has released a standard dealing with CSP, J-STD-012 "Implementation of Flip Chip and Chip Scale Technology" <LINK to IPC> [D1]. This standard contains technology overview and information on design considerations, material properties and processes, mounting and interconnection structures, assembly processes, requirements for reliability, and standardisation.

Although one of the advantages of CSPs compared to bare die assembling is the possibility to standardise, pitch and attachment site dimensions are still not standardised. Pitch and attachment site dimensions for grid array packages proposed by the Electronics Industry Association of Japan (EIAJ) is presented in Table D1.

Table D1. Proposed pitch and attachment site dimensions for grid array packages by the EIAJ.

Pitch (mm)	Attachment site diameter (mm)
0.4	0.25
0.5	0.30
0.65	0.40
0.8	0.50
1.0	

Tessera in USA has proposed 0.25, 0.50, 0.75, 1.00, and 1.25 mm as standard pitches and 0.10, 0.15, 0.20, 0.25, 0.30, and 0.35 mm as standard attachment site diameters for grid array packages.

For leaded packages, J-STD-012 prescribes that JEDEC's publication JEP-95 should be followed which recommend the following pitches: 0.2, 0.3, 0.4, 0.5, 0.63, and 0.65 mm.

New standards that need to be developed are defined in J-STD-012. These standards, include the following:

- Std No. 102: Mechanical outline Standard for Flip Chip or Chip Scale Configurations
- Std No. 103: Performance Standard for Flip Chip/Chip Scale Bumps
- Std No. 104: Test Methods for Flip Chip or Chip Scale Performance
- Std No. 105: Flip Chip/Chip Scale Carrier Tray Standard
- Std No. 106: Bare Dice as Flip Chip or Chip Scale Configuration Management Standard
- Std No. 107: Design Standard for Flip Chip and Chip Scale Mounting Structures
- Std No. 111: Design Standard for Flip Chip/Chip Scale Assembly Configuration
- Std No. 112: Standard for Flip Chip/Chip Scale Assembly Performance Requirements
- Std No. 113: Test Methods for Qualification and Evaluation of Flip Chip/Chip Scale Assemblies
- Std No. 114: Standard for Flip Chip/Chip Scale Assembly Rework and Repair Techniques
- Std No. 115: Flip Chip/Chip Scale Assembly Reliability Standard
- Std No. 120: Qualification and Performance Standard for Flux used in Flip Chip Assembly

Some of these are now available as proposals (see Section D4.3) <Link>

D1.6 Price

Only a few CSPs are in production today and then in low volume production. Therefore, it is difficult to get information of what the price will be for various CSPs. Furthermore, the large variations in construction of the various package types will also affect the production costs for the various packages. Many company forecast that the cost initially will be 10 to 50 % higher than conventional packages and that cost parity will be reached when they are produced in high volumes.