B. Flip-Chip Technology

B4. Level 4. References

B4.1 Recommended reading

D. Patterson, P. Elenius and J. Leal, "A Comparative Analysis – Solder deposition process and assembly wafer bumping – part I", EPP Printed Circuit Board, March 1998, 40 – 41.
D. Patterson, P. Elenius and J. Leal, "A Comparative Analysis – Solder deposition process and assembly wafer bumping – part II", EPP Printed Circuit Board, May 1998, 30 – 36.
D. Patterson, P. Elenius and J. Leal, "A Comparative Analysis – FC solder deposition, wafer bumping and assembly considerations – (III)", EPP Printed Circuit Board, August 1998, 29 – 31.
G. Schiebel, "A very promising technology – COB and flip chip processing with flexible SMD equipment – part I", EPP Printed Circuit Board, August 1997, 31-33.
G. Schiebel, "A very promising technology – COB and flip chip processing with SMD placement equipment – (II)", EPP Printed Circuit Board, October 1997, 32-36.
Flip Chip Technologies, ed. John H. Lau, McGraw-Hill, 1995, 565 pages.
John H. Lau and Yi-Hsin Pao, Solder Joint Reliability of BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies, McGraw-Hill, 1997, 408 pages.

B4.2 Flip chip literature

Bumping

J. Kaitila, P. Majander, J. Salonen and I. Suni, “Electroplated solder bumps for flip chip,” ISHM-Nordic 33rd Conference. Helsingör, 22 -25 Sept. 1996 (1996), pp. 98 - 103.
P. Annala, J. Kaitila, J. Salonen and I. Suni, “Electroplated solder alloys for flip chip interconnections,” 17th Nordic Semiconductor Meeting 17NSM. Trondheim, NO, 17 - 20 June 1996 (1996), pp. 115 - 8.
K. Kulojärvi and J. K. Kivilahti, “A New Under Bump Metallurgy for Solder Bump Flip Chip Applications,” 11th European Microelectronics Conference, Venice, 14 - 16 May 1997, Italy.
J. Salonen and J. Salmi, “A flip chip process based on electroplated solder bumps,” Physica Scripta. Vol. T54 (1994), pp. 230 - 3.

Reliability

J. H. Lau, “Solder Joint Reliability of Flip Chip and Plastic Ball Grid Array Assemblies Under Thermal, Mechanical, and Vibrational Conditions,” IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B, Vol. 19 Nov. 1996, 728-35.
J. H. Lau, “The Roles of DNP (Distance to Neutral Point) on Solder Joint Reliability of Area Array Assembies,” Soldering & Surface Mount Technology, No. 26, July 1997, 58-60.
R, Darveaux and K. Banerji, “Fatigue Analysis of Flip Chip Assemblies Using Thermal Stress Simulations and Coffin-Manson Relation,” Proc. 41st Electronic Components and Technology Conference 1991, ISBN 0780300130, 797-805.
A. Tuominen, A. Perttula and E. Ristolainen, “Characterization of flip chip joints,” Future Fab International Vol.1, Issue 4 (1997) 349-51.
A. Schubert, R. Dudek, B. Michel, H. Reichl and H. Jiang, “Materials Mechanics and Mechanical Reliability of Flip Chip Assemblies on Organic Substrates,” 1997 International Symposium on Advanced Packaging Materials p. 106-109.
K. Kulojärvi, V. Vuorinen and J. K. Kivilahti, “Effect of Dissolution and Intermetallic Formation on the Reliability of FC Joints,” ISHM-Nordic, Oslo (1997).

Heat transfer and performance issues

T-Y. Lee and M. Mahalingam, “Thermal Limits of Flip Chip Package – Experimentally Validated, CFD Supported Case Studies,” IEEE Trans. on Components, Packaging, and Manufacturing Technology – Part B, Vol 20, No. 1, February 1997, 94 – 103.

C. Bash and R. Blanco, “Improving Heat Transfer from a Flip-Chip Package,” Hewlett-Packard Journal, Aug. 1997, 121-5.

R. Sihlbom, M. Dernevik, Z. Lai, P. Starski and J. Liu, “Conductive Adhesives for High-Frequency Applications,” Proceedings of the First IEEE International Symposium on Polymeric Electronics Packaging, October 26-30 1997, Norrköping, Sweden, p.123-130.

Technologies and manufacturing issues

R. Aschenbrenner, R. Miessner and H. Reichl, “Adhesive Flip Chip Bonding on Flexible Substrates,” Proceedings of the First IEEE International Symposium on Polymeric Electronics Packaging, October 26-30 1997, Norrköping, Sweden. p.86-93.

Y. Tomura, Y. Bessho, T. Shiraishi, M. Itagaki, S. Yuhaku, T. Ishida and T. Ohbayashi, “Advanced Flip Chip Bonding Technique for MCM-L,” Pan Pacific Microelectronics Symposium, Proceedings of The technical Program, Honolulu, Hawaii, February 6-8, 1996, 125-30.

T. E. Adams, “Close look under flip chips,” EPP Test & Measurement, Aug. 1997, 58-59.

D. R. Gamota and C. M. Melton, “Encapsulant materials systems for flip-chip-on -board assemblies: addressing manufacturing issues,” Circuit World, 24/1 (1997) 7-12.

P. Kasulke, G. Azdasht, E. Zakel and H. Reichl, “Solder Ball Bumper (SBB) - A Flexible Equipment for FC, CSP, BGA and Printed Circuit Boards,”

J. Nave, E. Jung, C. Kallmayer, D. Lin, P. Kasulke, E. Zakel and H. Reichl, “A New Bumping Technique Using Ball and Wedge Bumping for Manufacturing of Hard Core Solder Bumps,”

G. Azdasht, P. Kasulke, E. Jung, E. Zakel and H. Reichl, “A New CSP-Technology based on Chip on Flex,”

J. Salonen and J. Salmi, “Test chip and process design for evaluating flip chip technology,” Proc. 1st International Symposium on Flip Chip Technology. San Jose, CA, 15 - 17 Feb. 1994 (1994), pp. 230 - 3.

T. Jaakola, J. Lenkkeri and J. Vähäkangas, “Flip-chip joining utilizing gold stud bumps,” 34th ISHM-Nordic Conference. Oslo, NO, 21 -24 September 1997 (1997), pp. 5 - 12.

T. Laine-Ylijoki and J. Kivilahti, “SnPb-Flip Chip on Pd-coated Substrates,” The Proc. of the International Workshop “Flip Chip and Ball Grid Arrays” (org. Fraunhofer-Institute-IZM), 13 - 15 November 1995, Berlin, Germany.

Markets

Flipped out over flip chip, IPC Review, January 1998, 1,15-16.

K. Boustedt and P. Hedemalm, The Nordic Flip Chip Project, ´95 Flip Chip, BGA, TAB & AP Symposium, p. 294 – 299.

Flip chip joining using adhesives

O. Rusanen, V. Pennanen and A. Björklöf, “The use of thermosetting and thermoplastic isotropically conductive adhesives in flip chip bonding,” Proceedings of the 33rd ISHM-Nordic Conference. Helsingör, DK, 22 -25 Sept. 1996 (1996), pp. 184 - 91.

V. Pennanen, O. Rusanen and A. Björklöf, “The mechanical strength of smart cards made by isotropic adhesive bonded flip chip,” Adhesives in Electronics `96. 2nd International Conference on Adhesive Joining and Coating Technology in Electronics Manufacturing. Stockholm, 3 - 5 June 1996, Sveriges Verkstadsindustrier. Stockholm Proceedings (1996), pp. 410 - 13.

V. Pennanen and O. Rusanen, “Testing the reliability of flip chip joining with isotropically conductive adhesives,” Journal of Electronics Manufacturing, 1998 (accepted for publication).

O. Rusanen, K. Keränen, M. Blomberg and A. Lehto, “Adhesive Flip Chip Bonding in a Miniaturised Spectrometer, Journal of Electronics Manufacturing,” 1998 (accepted for publication).

K. Puhakka, K. Kulojärvi, P. Savolainen and J. Kivilahti, “Bonding Flexible Circuits and Flip Chips with Solder-filled Z-adhesives,” Non-conductive adhesives and Fusible Coatings, Intl. Journal of Microelectronic Packaging (in print).

J. Kivilahti and P. Savolainen, “Design and Modelling Solder-filled ACAs for Flip Chip and Flexible Circuit Applications,” The Art and Science of Adhesives in Electronics (Ed. by J.Liu), Electrochemical Publications Limited, 1997.

P. Savolainen and J. Kivilahti, “Boundary Conditions for Using Anisotropic Adhesives for Flip-Chip Bonding,” The Proc. of the Second European Conference on Microelectronics Packaging, 1 - 3 February 1996, Essen, Germany.

J. Kivilahti and P. Savolainen, “Anisotropic Adhesives for Flip Chip Bonding,” J. of Electronics Manufacturing, vol. 5, No. 4 (1995), pp. 245 - 52.
K. Kulojärvi and J. Kivilahti, “Flip Chip Assembly with Non-Conductive Adhesives and Fusible Coatings,” The Proc. of the International Workshop “Flip Chip and Ball Grid Arrays” (org. Fraunhofer-Institute-IZM), 13 - 15 November 1995, Berlin, Germany.
J. Kivilahti, “Anisotropic Adhesives for Flip-Chip Bonding,” the Proc. of the International Symposium on Conductive Adhesives in Electronics Packaging, 5 September 1995, Philips Center for Manufacturing Technology, Philips, Eindhoven, The Netherlands, pp. 59 - 67 (Invited).

B4.3 List of key conferences

Flip Chip Technologies Volume 1, 2 Day Tutorial, Munich, Germany, Nov. 11-12, 1996, Pac Tech - Packaging Technologies GmbH, Fraunhofer - Institut für Zuverlässigkeit und Mikrointegration.
1st Netpack Meeting, December 15 1993, Brussels.
2nd Netpack Meeting, June 7, 1994, Windsor.
3rd Netpack Meeting, October 20, 1994, Berlin.
4th Netpack Meeting, May 17, 1995, Copenhagen.
5th Netpack Meeting, April 2, 1996, Paris.
6th Netpack Meeting, September 18, 1996, Berlin.
Netpack Who is who in European Packaging, Fraunhofer Einrichtung, Institut für Zuverlässigkeit und Mikrointegration, 1995, 56 pages + 18 appendices.
10th European Microelectronics Conference, Copenhagen, 14-17 May 1995.
11th European Microelectronics Conference - EMC ´97, 14-16 May 1997.
Area Array Packaging Technologies, Workshop on Flip Chip and Ball Grid Arrays, November 13-15, 1995, Berlin, Fraunhofer- Institute for Reliability and Microintegration

B4.4 Standards

Pending ANSI Approval:

J-STD-012 Implementation of Flip Chip and Chip Scale Technology - Chair, Ray Prasad Concultancy Group, Jan 1996.

New Standards under development as defined in J-STD-012

Std No. 101: Semiconductor Design Standard for Flip Chip Applications.
Std No. 102: Mechanical Outline Standard for Flip Chip or Chip Scale Configurations.
Std No. 103: Performance Standard for Flip Chip/Chip Scale Bumps.
Std No. 104: Test Methods for Flip Chip or Chip Scale Performance.
Std No. 105: Flip Chip/Chip Scale Carrier Tray Standard.
Std No. 106: Bare Dice as Flip Chip or Chip Scale Configuration Management Standard.
Std No. 107: Design Standard for Flip Chip and Chip Scale Mounting Structures.
Std No. 108: Qualification and Performance Standard for Flip Chip Organic Mounting Structures.
Std No. 109: Qualification and Performance Standard for Flip Chip Inorganic Mounting Structures.
Std No. 110: Test Methods for Qualification and Evaluation of Flip Chip Mounting Structures.
Std No. 111: Design Standard for Flip Chip/Chip Scale Assembly Configuration.
Std No. 112: Standard for Flip Chip/Chip Scale Assembly Performance Requirements.
Std No. 113: Test Methods for Qualification and Evaluation of Flip Chip/Chip Scale Assemblies.
Std No. 114: Standard for Flip Chip/Chip Scale Assembly Rework and Repair Techniques.
Std No. 115: Flip Chip/Chip Scale Assembly Reliability Standard.
Std No. 116: Qualification and Performance of Flip Chip Underfill Materials.
Std No. 117: Qualification and Performance of Flip Chip Passivation Materials.
Std No. 118: Qualification and Performance of Flip Chip Encapsulation Materials.
Std No. 119: Qualification and Performance Standard for Adhesives Used in Flip Chip Assembly.
Std No. 120: Qualification and Performance Standard for Flux Used in Flip Chip Assembly.

B4.5 References