B. Flip-Chip Technology

B1. Level 1. Introduction to Flip-Chip techniques

B1.1 Why flip-chip?

In the development of packaging of electronics the aim is to lower cost, increase the packaging density, improve the performance while still maintaining or even improving the reliability of the circuits. The concept of flip-chip process where the semiconductor chip is assembled face down onto circuit board is ideal for size considerations, because there is no extra area needed for contacting on the sides of the component. The performance in high frequency applications is superior to other interconnection methods, because the length of the connection path is minimised. Also reliability is better than with packaged components due to decreased number of connections. In flip-chip joining there is only one level of connections between the chip and the circuit board.

Potentially flip chip technology is cheaper than wire bonding because bonding of all connections takes place simultaneously whereas with wire bonding one bond is made at a time. In practise, however, this price benefit is not always achieved due to immature processes, e.g. the cost of die bumping with current processes can be significant, especially in low volumes.

Flip-chip joining is not a new technology. The technology has been driven by IBM for mainframe computer applications. Many millions of flip chips have been processed by IBM on ceramic substrates since the end of 60’s. At the beginning of 70’s the automotive industry also began to use flip chips on ceramics. Today flip-chips are widely used for watches, mobile phones, portable communicators, disk drives, hearing aids, LCD displays, automotive engine controllers as well as the main frame computers. The number of flip chips assembled was over 500 million in year 1995 and close to 600 million flip chips were consumed 1997 [B1].

B1.2 General benefits/disadvantages

Advantages:
- Smaller size: Smaller IC footprint (only about 5% of that of packaged IC e.g. quad flat pack), reduced height and weight.
- Increased functionality: The use of flip chips allow an increase in the number of I/O. I/O is not limited to the perimeter of the chip as in wire bonding. An area array pad layout enables more signal, power and ground connections in less space. A flip chip can easily handle more than 400 pads.
- Improved performance: Short interconnect delivers low inductance, resistance and capacitance, small electrical delays, good high frequency characteristics, thermal path from the back side of the die.
- Improved reliability: Epoxy underfill in large chips ensures high reliability. Flip-chips can reduce the number connections per pin from three to one.
- Improved thermal capabilities: Because flip chips are not encapsulated, the back side of the chip can be used for efficient cooling.
- Low cost: Batch bumping process, cost of bumping decreases, cost reductions in the underfill-process.
Figure B1. Comparison of the number of I/O vs. chip size between area array and perimeter array pad arrangement for pitches of 0.2 mm and 0.4 mm.

Disadvantages:
- Difficult testing of bare dies.
- Limited availability of bumped chips.
- Challenge for PCB technology as pitches become very fine and bump counts are high.
- For inspection of hidden joints an X-ray equipment is needed.
- Weak process compatibility with SMT.
- Handling of bare chips is difficult.
- High assembly accuracy needed.
- With present day materials underfilling process with a considerable curing time is needed.
- Low reliability for some substrates.
- Repairing is difficult or impossible.

B1.3 Relative cost comparison

The cost of flip chip technology can be divided into bumping cost and assembly process cost. Die bumping costs are dependent on wafer size, number of dies per wafer, wafer yield and volume. The assembly processes for the most common flip chip technology include pick and place together with flux application, reflow and cleaning as well as underfill process and its curing. The cost of the necessary equipment and floor space, the capacity of the equipment and its compatibility with other manufacturing processes are also important factors having influence on the economy of the technology for particular product. The substrate has also an important impact on the packaging costs. The cost of substrate depends e.g. on via sizes, layer count, line width and spaces, die pad pitch, flatness requirements, material type, panelization optimisation and the fabrication process.

In the case of manufacturing of 300 - 400 I/O BGA packages in the volume of 1 million per month the capital cost of flip chip process is less than half of the corresponding cost for wire bonding technology and the floor space needed is also only about one half of that for wire bonding technology.

The cost of bumping with solder bumps using common batch processes is practically independent of the wafer size. The costs per die are therefore strongly dependent on the number of good dies obtained from one wafer. An order of magnitude for wafer bumping in high volume production is $85 per wafer. For the case of 10 mm die on 8 inch wafer and yield of 90% the bumping cost per die is $0.37.

The cost of wire bonding process increases with increasing number of I/O’s while the cost of flip chip process is practically independent of the I/O count. For very high I/O numbers the flip chip process is the only choice.
Wire bonding, which is a mature technology, costs about $0.03 per pin, based on a 500 I/O device. The cost to bump a 200 mm with the evaporative process is around $200, sputtering and plating comes in at around $100, and electroless nickel bumping cost projections are below $50 [B1].

B1.4 Availability of components

A precondition for using flip chip technique is availability of bumped chips or alternatively known good bare dies when bumping is done separately. The use of solder bumping is the most common process alternative. Many chip houses already deliver solder bumped dies <LINK TO http://www.imec.be/kgd/>. Solder bumping which is a wafer level process, needs big and expensive facilities. Therefore it is not convenient to have inhouse processing facilities for solder bumping. There are also specialised companies making services of solder bumping.

The situation with the availability of solder bumped and tested chips for flip chip bonding is still not satisfactory. Flip chip bonding knowledge is spreading slowly and as an additional production step in wafer manufacturing the known good die (KGD) issue is still causing a certain degree of uncertainty on the user side [B2].

B1.5 How mature is the technology?

Although flip chip technology has been used already for about 30 years, it is still in quite limited use. It has many technical variations which have very different levels of maturity and fairly restricted availability. The flip chip technology using solder joining is already in a fairly mature state. The limitations are at least partly related to the limited availability of bumped components and limited compatibility with available SMD processing equipment.

B1.6 Short description of each flip chip process

There are many different alternative processes used for flip-chip joining. A common feature of the joined structures is that the chip is lying face down to the substrate and the connections between the chip and the substrate are made using bumps of electrically conducting material. Cross sections of flip chip joints without and with underfill material are shown in Figure B2. Examples of the different types of flip chip joints are schematically shown in Figure B3.

Figure B2. Cross sections of flip chip joints without and with underfill material.
B1.6.1 Flip chip process by solder joining. <LINK TO B2.1>

In flip chip soldering process solder bumped chips are soldered onto the circuit board. Solder is usually, but not always, deposited also on to the substrate pad areas. For fine pitch applications, solder can be deposited e.g. by electroplating, solder ink jet or solid solder deposition. Tacky flux is applied to the solder contact areas either by dipping the chip into a flux reservoir or by dispensing flux onto the substrate. For coarse pitch applications (>0.4 mm) solder paste is deposited on the substrate by stencil printing. The bumps of chips are placed into the tacky paste and they are reflowed in an oven. After the reflow process cleaning of the flux is preferred. The underfill material is applied by dispensing along one or two sides of the chip, from where the low viscosity epoxy is drawn by capillary forces into the space between the chip and substrate. Finally the underfill is cured by heat. Repairing of the flip chip joint is usually impossible after the underfill process. Therefore testing must be done after reflow and before the underfill application. The steps of flip chip soldering process are:

- die preparing (testing, bumping, dicing)
- substrate preparing (flux application or solder paste printing)
- pick, alignment and place
- reflow soldering
- cleaning of flux residues (optional)
- underfill dispensing
- underfill curing.

Figure B3. Examples of different types of flip chip joints.
B1.6.2 Flip chip joining by thermocompression. <LINK TO B2.2>

In the thermocompression bonding process, the bumps of the chip are bonded to the pads on the substrate by force and heat applied from an end effector. The process requires gold bumps on the chip or the substrate and a correspondingly bondable surface (e.g., gold, aluminium). The bonding temperature is usually high, e.g., 300 °C for gold bonding, to soften the material and increase the diffusion bonding process. The bonding force can be up to 1 N for an 80μm diameter bump. Due to the required high bonding force and temperature, the process is limited to rigid substrates such as alumina or silicon. Additionally, the substrates must have a high planarity. A bonder with high accuracy in the parallelism alignment is required. In order to avoid pre-damaging of the semiconductor material, the bonding force must be applied with a gradient.
B1.6.3 Flip chip thermosonic joining

The thermocompression bonding process can be made more efficient by using ultrasonic power to speed up the welding process. Ultrasonic energy is transferred to the bonding area from the pick-up tool through the back surface of the chip. The thermosonic bonding introduces ultrasonic energy that softens the bonding material and makes it vulnerable to plastic deformation. The main benefit of the method compared to thermocompression is lower bonding temperature and shorter processing time. One potential problem associated with thermosonic bonding is silicon cratering. It is generally believed that such damage results from excessive ultrasonic vibration.

B1.6.4 Flip chip joining using adhesives (isotropic, anisotropic, nonconductive)

Conductive adhesives have become a viable alternative to tin-lead solders also in flip chip joining. Adhesively bonded flip chip combines the advantages of thin structures and cost efficiency. The advantages of conductive adhesives include ease of processing, low curing temperatures, and elimination of the need to clean after the bonding process. Anisotropically conductive adhesives have also the ability to connect fine pitch devices. Figure B7 shows a schematic drawing of flip chip bonding with isotropically and anisotropically conductive adhesives (ICAs and ACAs). Also nonconductive adhesives can be used for flip chip bonding, in this case the joint surfaces are forced into intimate contact by the adhesive between the component and substrate.

Isotropically conductive adhesive

Component

Polymer filled with conducting (metal)particles such as silver

Substrate

Anisotropically conductive adhesive

Component

Polymer

Conducting particles such as nickel plated polymer ball

Substrate

Figure B6. Principles of flip chip joining by thermocompression and thermosonic processes.

Figure B7. Schematic drawings of flip chip joints made with conductive adhesives.

Isotropically conductive adhesives are pastes of polymer resin that are filled with conducting particles to a content that assures conductivity in all directions. Generally, the polymer resin is epoxy and conducting particles are silver. Anisotropically conductive adhesives are pastes or films of thermoplastics or b-stage
epoxies. They are filled with metal particles or metal coated polymer spheres to a content that assures electrical insulation in all directions before bonding. After bonding the adhesive becomes electrically conductive in z-direction. The metal particles are typically nickel or gold and these metals are also used to coat polymer spheres.

B1.7 Reliability
The different flip chip processes have different aspects concerning the reliability. However, one key factor which has drastically increased the reliability of flip chip structures against temperature variations is the use of underfiller between the chip and the circuit board which, when properly selected and applied, may increase the reliability by more than one decade. The underfill materials, usually filled epoxies, are stiff enough to take part of the forces developed by different thermal expansion coefficients of the chip and substrate. An underfill material also protects the face of the chip against moisture and impurities and makes the structure mechanically stronger.

B1.8 Testing [LINK TO B2.1 TESTING PARAGRAPHS]
The reason for testing is to assure the functionality of the components before and after the flip chip process. The flip chip joined structure should be tested before underfill process when the repairing is still possible.

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